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[54] **ELECTRICALLY PROGRAMMABLE AND ERASABLE NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND OPERATING METHOD THEREFOR**

[75] Inventors: **Shinichi Kobayashi; Yasushi Terada; Yoshikazu Miyawaki; Takeshi Nakayama; Tomoshi Futatsuya; Natsuo Ajika; Yuichi Kunori; Hiroshi Onoda; Atsushi Fukumoto; Makoto Ohi,** all of Hyogo-ken, Japan

[73] Assignee: **Mitsubishi Denki Kabushiki Kaisha,** Tokyo, Japan

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[52] **U.S. Cl.** **365/63**; 365/185.11; 365/185.13; 365/185.17

[58] **Field of Search** 365/185.01, 185.11, 365/185.13, 185.12, 185.17; 8/230.06, 63, 52; 257/315, 316, 317, 318

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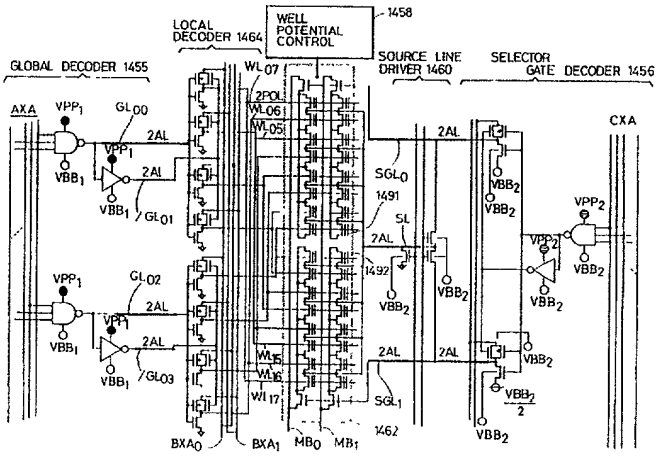
Primary Examiner—Vu A. Le

Attorney, Agent, or Firm—McDermott, Will & Emery

[57] **ABSTRACT**

In erasing, electrons are simultaneously injected into floating gates from sources of a plurality of memory cells. Thus, the threshold voltages of the plurality of memory cells are increased. In programming, electrons are emitted from a floating gate of a selected memory cell to a drain. Thus, the threshold voltage of the selected memory cell is reduced.

2 Claims, 124 Drawing Sheets



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